CLAIMS

What is claimed is:

1. A quadrature clock generating apparatus comprising:

a clock generator providing a double clock having a frequency that is twice that of a received reference clock;

divider circuitry coupled to provide an alignment signal with a frequency half that of the double clock; and

a recovery circuit for recovering a first clock and a second clock from the double clock in accordance with the alignment signal, wherein the first and second clocks have substantially a 90° phase difference.

2. The apparatus of claim 1 wherein the recovery circuit comprises:

a first flip-flop receiving the alignment signal, wherein the first flip-flop is clocked by the double clock to provide the first clock; and

a second flip-flop receiving the first clock, wherein the second flip-flop is clocked by an inverted double clock to provide the second clock.

3. The apparatus of claim 2 wherein each of the first and second flip-flops is a D-type flip-flop.

4. The apparatus of claim 1 wherein the clock generator is a phase locked loop circuit.

5. The apparatus of claim 1 wherein the divider circuitry further comprises:

an inverter coupled to provide an inverted double clock; and

a divider coupled to divide the inverted double clock to provide the alignment signal.

6. The apparatus of claim 1 wherein the clock generator, divider, and recovery circuitry reside on a same integrated circuit die.

7. The apparatus of claim 6 wherein the clock generator, divider and recovery circuitry are formed as a metal oxide semiconductor field effect transistor (MOSFET) integrated circuit.

8. A quadrature clock generation apparatus, comprising:

a clock generator providing a double clock having a frequency twice that of a received reference clock;

divider circuitry coupled to provide an alignment signal having a frequency half that of the double clock; and

a plurality of recovery circuits, each recovery circuit recovering an associated first clock and an associated second clock from the double clock in accordance with the alignment signal, wherein the first and second clocks associated with each recovery circuit have substantially a 90° phase difference.

9. The apparatus of claim 8 wherein the first clock associated with any recovery circuit is substantially synchronized with the first clock associated with any other recovery circuit.

10. The apparatus of claim 8 wherein each recovery circuit comprises:

a first flip-flop receiving the alignment signal, wherein the first flip-flop is clocked by the double clock to provide the first clock; and

a second flip-flop receiving the first clock, wherein the second flip-flop is clocked by an inverted double clock to provide the second clock.

11. The apparatus of claim 10 wherein each of the first and second flip-flops is a D-type flip-flop.

12. The apparatus of claim 8 wherein the clock generator is a phase locked loop circuit, wherein the first and second clocks have a same frequency as the reference clock, wherein the first clock is synchronized with the reference clock.

13. The apparatus of claim 8 wherein the divider circuitry further comprises:

an inverter coupled to provide an inverted double clock from the double clock; and

a divider coupled to divide the inverted double clock to provide the alignment signal.

14. The apparatus of claim 8 wherein the clock generator, divider, and recovery circuitry reside on a same integrated circuit die.

15. The apparatus of claim 14 wherein the clock generator, divider and recovery circuitry are formed as a metal oxide semiconductor field effect transistor (MOSFET) integrated circuit.

16. A method of generating a quadrature clock, comprising:

generating a double clock having a frequency twice that of a received reference clock;

generating an alignment signal having a frequency half that of the double clock;

deriving a first clock from the double clock in accordance with the alignment signal; and

deriving the second clock from the first clock, wherein the first and second clocks have substantially a 90° phase difference.

17. The method of claim 16 wherein deriving the first clock includes latching the alignment signal in accordance with the double clock to provide the first clock, wherein deriving the second clock includes latching the first clock in accordance with an inverted double clock to provide the second clock.

18. The method of claim 16 further comprising:

providing differential distribution of the double clock.

19. The method of claim 16 wherein the alignment signal corresponds to an inverted double clock divided by two.

20. The method of claim 16 wherein deriving the first clock further comprises providing the alignment signal to a first latch, wherein the first latch is clocked by the double clock to provide the first clock.